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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
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ART UNIT	PAPER NUMBER
2133	6

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/859,659	WALTON, JOHN K.	
	Examiner	Art Unit	
	Marshall S Eng	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☒ Claim(s) *1,3,5,7 and 9-14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 May 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☒ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Priority

1.1 If applicant desires priority under 35 U.S.C. 120 based upon a previously filed application, specific reference to the earlier filed application must be made in the instant application. For benefit claims under 35 U.S.C. 120, 121 or 365(c), the reference must include the relationship (i.e., continuation, divisional, or continuation-in-part) of the applications. This should appear as the first sentence of the specification following the title, preferably as a separate paragraph unless it appears in an application data sheet. The status of nonprovisional parent application(s) (whether patented or abandoned) should also be included. If a parent application has become a patent, the expression "now Patent No. _____" should follow the filing date of the parent application. If a parent application has become abandoned, the expression "now abandoned" should follow the filing date of the parent application.

If the application is a utility or plant application filed under 35 U.S.C. 111(a) on or after November 29, 2000, the specific reference must be submitted during the pendency of the application and within the later of four months from the actual filing date of the application or sixteen months from the filing date of the prior application. If the application is a utility or plant application which entered the national stage from an international application filed on or after November 29, 2000, after compliance with 35 U.S.C. 371, the specific reference must be submitted during the pendency of the application and within the later of four months from the date on which the national stage commenced under 35 U.S.C. 371(b) or (f) or sixteen months from the filing date of the prior application. See 37 CFR 1.78(a)(2)(ii) and (a)(5)(ii). This time period is not

extendable and a failure to submit the reference required by 35 U.S.C. 119(e) and/or 120, where applicable, within this time period is considered a waiver of any benefit of such prior application(s) under 35 U.S.C. 119(e), 120, 121 and 365(c). A priority claim filed after the required time period may be accepted if it is accompanied by a grantable petition to accept an unintentionally delayed claim for priority under 35 U.S.C. 119(e), 120, 121 and 365(c). The petition must be accompanied by (1) the reference required by 35 U.S.C. 120 or 119(e) and 37 CFR 1.78(a)(2) or (a)(5) to the prior application (unless previously submitted), (2) a surcharge under 37 CFR 1.17(t), and (3) a statement that the entire delay between the date the claim was due under 37 CFR 1.78(a)(2) or (a)(5) and the date the claim was filed was unintentional. The Director may require additional information where there is a question whether the delay was unintentional. The petition should be addressed to: Mail Stop Petition, Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

1.2 Specifically, the Specifications claims benefit under 35 U.S.C 120, while the declaration does not make not note of this claim. A declaration claiming benefit of the cross-referenced applications is required. Further, as noted in the above paragraphs:

> For benefit claims under 35 U.S.C. 120, 121 or 365(c), the reference must include the relationship (i.e., continuation, divisional, or continuation-in-part) of the applications.

In the attempted claim for benefit under 35 U.S.C 120, the applicant lists the relationship as co-pending.

Oath/Declaration

2.1 The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

The oath or declaration is defective because:

The applicant is attempting to claim benefit under 35 U.S.C. 120 in the specifications (in pre-amendment A) but fails to claim the benefit in the declaration.

Drawings

3.1 The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: references 300, 190 sub 1 – 190 sub 8, and 210 sub 1 – 210 sub 8 of Figures 3 and 4, as mentioned on page 12 of the specifications.

3.2 The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "22" has been used to designate both memory board and global memory cache on lines 17 and 18 of page 12.

3.3 The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: 320' of Figure 5.

3.4 A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

4.1 The disclosure is objected to because of the following informalities: the word "store" in the phrase "wherein data is read from, and store in, a memory" should be "stored." All occurrences, for example on line 1 of the abstract and line 6 of page 5, within the specifications (and claims, as noted below) should be corrected.

4.2 The abstract of the disclosure is objected to because the abstract describes, completely, the invention of claims 1 and 2. While the abstract does teach of the nature and gist of the technical disclosure, it only teaches of the nature of claims 1 and 2. A more general abstract encompassing the disclosure and all of the claims is suggested.

Appropriate correction is required.

Claim Objections

5.1 Claims 1, 3, 5, 7, 9, 11, and 13 are objected to because of the following informalities: the phrase "store in" in line 1 of all of the claims should be "stored in."

5.2 Claims 3, 5, 7, 9, 11, and 13 are further objected to because of the following informalities: the phrase "same or different" when describing the conditions that cause a NOOP is unclear. It is not clear why, if both signals in the checker are the same that a NOOP would be generated.

5.3 Claim 7 is further objected to because of the following informalities: the word "from" is missing from the phrase "primary section (from) the address/control" on line 10.

5.4 Claim 7 is further objected to because of the following informalities: the phrase "from the address/control portion at the first port and" is missing in line 13. It should appear between the words "primary section" and "a digital word."

5.5 The specification is further objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: the phrase "parity bit generated by **the** first parity generator of the secondary section" on line 11 of claim 3 lacks antecedent basis for the first parity generator of the secondary section. The "**the**" should be replaced by an "**a**."

5.6 The specification is further objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: the phrase "to the memory if **the** digital word" on line 9 of claim 5 lacks antecedent basis for the digital word. The "**the**" should be replaced by an "**a**."

5.7 The specification is further objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: the phrase "and **the** digital word" on line 11 of claim 5 lacks antecedent basis for the digital word. The "**the**" should be replaced by an "**a**."

5.8 The specification is further objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: the phrase "parity bit generated by **the** first parity generator of the secondary section" on line 11 of claim 7 lacks antecedent basis for the first parity generator of the secondary section. The "**the**" should be replaced by an "**a**."

5.9 The specification is further objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o).

Correction of the following is required: the phrase "the first port and **the** write data port" on line 6 of claim 9 lacks antecedent basis for the write data port. The "**the**" should be replaced by an "**a**."

5.10 The specification is further objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: the phrase "**the** selector" on line 3 of claim 10 lacks antecedent basis for the selector. The "**the**" should be replaced by an "**a**."

5.11 The specification is further objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: the phrase "**the** inverter" on line 23 of claim 11 lacks antecedent basis for the inverter. The "**the**" should be replaced by an "**a**."

5.12 The specification is further objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: the phrase "**the** selector" on line 3 of claim 12 lacks antecedent basis for the selector. The "**the**" should be replaced by an "**a**."

5.13 The specification is further objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: the phrase "**the** inverted parity bit" on line 30 of claim 13 and on line 3 of claim 14 lacks antecedent basis for the selector. The "**the**" should be replaced by an "**an**."

5.14 Claims 1-8 are objected to because of the following informalities: the term "NOOP" is not defined in its first instance. In the first instance (Claim 1), "NOOP"

should be fully expressed as "no-op" or "no-operation" and then note that "NOOP" will be used as its abbreviation.

Appropriate corrections are required.

Claim Rejections - 35 USC § 103

6.1 The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6.2 Claim(s) 1-14 is/are rejected under 35 U.S.C. 103(a) as being unpatentable over Richter U.S. Patent No. 4,245,344 (hereinafter Richter) in view of Cloonan U.S. Patent No. 5,566,193 (hereinafter Cloonan).

As per claim 1,

Richter substantially teaches of a system where data is read from and stored in a memory, see abstract line 1, with the data having address/control portion, see the command address description in column 3, lines 20-35. Richter further teaches of a pair of controller sections that implement identical logic that controls the transfer of data into the memory, see column 5, lines 5-20. The parity checkers 127 and 128 of Figure 4 feed the control section 120 with the parity bits. The examiner is reading the parity checkers as section of a controller, where the controller includes the control 120 and the two parity checkers 127 and 128. The claimed controller is an obvious inclusion of the two parity checkers and the controller into a single unit.

Further, Richter teaches of a write data port of a control section being connected to the memory, see line 164 of Figure 4, which controls the writing to the memory of the data in register 169. Richter further teaches of, when an input error is detected (i.e. the received signals or their parity checks are not equal), the control (or the checker) insuring that the memory module (104 of Figure 4) does not utilize the signals received by completing execution of an instruction (i.e. a NOOP instruction), see column 6, lines 20-27.

Richter does not explicitly teach of the first port being connected to both sections. Nonetheless, Richter does teach of preventing the use of erroneous signals by comparing the parity of the two signals and of preventing the use signals when an error is detected (i.e. the results of the parity checks do not match).

Cloonan, in an analogous art, teaches of a first port (reference 42 of Figure 2) feeding into/connected to two transmitters 60 and 80, which in turn feeds out to output bus 120. Cloonan also explicitly teaches that both copies of the data are generated from the same signal, i.e. input 42 of Figure 2. Further, Cloonan explicitly teaches that the same parity checks are performed and then the results of the words received in parallel are compared (and are identical if no error has occurred), see column 6, lines 1-8.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to adapt the memory of Richter to include the teachings of Cloonan. This modification would have been obvious because one of ordinary skill in the art would have been motivated by the suggestion provided by Cloonan to provide

serial communication of data at very high actual and effective data rates with high probabilities of detecting errors, see abstract, lines 1-3. Also, both Richter and Cloonan teach of redundant memory/data transfers that involve generating parity checks to determine the validity of the received data.

As per claim 2,

Both of the above cited references, Richter and Cloonan, substantially teach, as combined above in claim 1, the limitations of claim 2.

With respect to the limitations of claim 2, Richter teaches of preventing the writing of data to memory when an error is detected, see column 6, lines 25-35. Further, Richter teaches of insuring that the memory module (104 of Figure 4) does not utilize the signals received by completing execution of an instruction (i.e. a NOOP instruction), see column 6, lines 20-27. While Richter does not explicitly teach of the NOOP command causing the storage to be inhibited, Richter does suggest that when an error is detected, an instruction causes the storage to be inhibited. Further, a NOOP command is a command in which the instruction is to do nothing. In other words a NOOP command simply tells the device receiving the instruction to do nothing. The claimed limitations, however, read that a NOOP instruction is used to produce a certain action/desired output. Therefore the Examiner is viewing the NOOP instruction simply as an instruction causing the memory/data to not be written to memory. Once read in this light, it is clear that Richter teaches of a issuing an instruction to inhibit the writing to memory of data once the data is found to have an error.

As per claim 3,

Richter substantially teaches of a system where data is read from and stored in a memory, see abstract line 1, with the data having address/control portion, see the command address description in column 3, lines 20-35. Richter further teaches of a pair of controller sections that implement identical logic that controls the transfer of data into the memory, see column 5, lines 5-20. The parity checkers 127 and 128 of Figure 4 feed the control section 120 with the parity bits. The examiner is reading the parity checkers as section of a controller, where the controller includes the control 120 and the two parity checkers 127 and 128. The claimed controller is an obvious inclusion of the two parity checkers and the controller into a single unit.

Further, Richter teaches or write data port of a control section being connected to the memory, see line 164 of Figure 4, which controls the writing to the memory of the data in register 169. Richter further teaches of, when an input error is detected (i.e. the parity checks aren't equal), the control (or the checker) ensuring that the memory module (104 of Figure 4) does not utilize the signals received by completing execution of an instruction (i.e. a NOOP instruction), see column 6, lines 20-27.

Richter does not explicitly teach of the first port being connected to both sections or specifically of the parity of the address/control portion being used. Nonetheless, Richter does teach of preventing the use of erroneous signals by comparing the parity of the two signals and of preventing the use signals when an error is detected (i.e. the results of the parity checks do not match).

Cloonan, in an analogous art, teaches of a first port (reference 42 of Figure 2) feeding into/connected to two transmitters 60 and 80, which in turn feeds out to output

bus 120. Cloonan also explicitly teaches that both copies of the data are generated from the same signal, i.e. input 42 of Figure 2. Further, Cloonan explicitly teaches that the same parity checks are performed and then the results of the words received in parallel are compared (and are identical if no error has occurred), see column 6, lines 1-8.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to adapt the memory of Richter to include the teachings of Cloonan. This modification would have been obvious because one of ordinary skill in the art would have been motivated by the suggestion provided by Cloonan to provide serial communication of data at very high actual and effective data rates with high probabilities of detecting errors, see abstract, lines 1-3. Both Richter and Cloonan teach of redundant memory/data transfers that involve generating parity checks to determine the validity of the received data.

Further, it would have been obvious to one of ordinary skill in the art to use the parity of a specific part of received data to determine if two received packets are without error. Specifically, it is not uncommon for two packets of data to have the same payload with different destinations. In this case, it would be obvious to one of ordinary skill to want to use the parity of the address section only to determine the validity of received packets.

As per claim 4,

Both of the above cited references, Richter and Cloonan, substantially teach, as combined above in claim 3, the limitations of claim 4.

With respect to the limitations of claim 2, Richter teaches of preventing the writing of data to memory when an error is detected, see column 6, lines 25-35. Further, Richter teaches of insuring that the memory module (104 of Figure 4) does not utilize the signals received by completing execution of an instruction (i.e. a NOOP instruction), see column 6, lines 20-27. While Richter does not explicitly teach of the NOOP command causing the storage to be inhibited, Richter does suggest that when an error is detected, an instruction causes the storage to be inhibited. Further, a NOOP command is a command in which the instruction is to do nothing. In other words a NOOP command simply tells the device receiving the instruction to do nothing. The claimed limitations, however, read that a NOOP instruction is used to produce a certain action/desired output. Therefore the Examiner is viewing the NOOP instruction simply as an instruction causing the memory/data to not be written to memory. Once read in this light, it is clear that Richter teaches of a issuing an instruction to inhibit the writing to memory of data once the data is found to have an error.

As per claim 5,

Richter substantially teaches of a system where data is read from and stored in a memory, see abstract line 1, with the data having address/control portion, see the command address description in column 3, lines 20-35. Richter further teaches of a pair of controller sections that implement identical logic that controls the transfer of data into the memory, see column 5, lines 5-20. The parity checkers 127 and 128 of Figure 4 feed the control section 120 with the parity bits. The examiner is reading the parity checkers as section of a controller, where the controller includes the control 120 and the

two parity checkers 127 and 128. The claimed controller is an obvious inclusion of the two parity checkers and the controller into a single unit.

Further, Richter teaches or write data port of a control section being connected to the memory, see line 164 of Figure 4, which controls the writing to the memory of the data in register 169. Richter further teaches of, when an input error is detected (i.e. the parity checks aren't equal), the control (or the checker) ensuring that the memory module (104 of Figure 4) does not utilize the signals received by completing execution of an instruction (i.e. a NOOP instruction), see column 6, lines 20-27.

Richter does not explicitly teach of the first port being connected to both sections or specifically of the parity of the entire digital word being used. Nonetheless, Richter does teach of preventing the use of erroneous signals by comparing the parity of the two signals and of preventing the use signals when an error is detected (i.e. the results of the parity checks do not match).

Cloonan, in an analogous art, teaches of a first port (reference 42 of Figure 2) feeding into/connected to two transmitters 60 and 80, which in turn feeds out to output bus 120. Cloonan also explicitly teaches that both copies of the data are generated from the same signal, i.e. input 42 of Figure 2. Further, Cloonan explicitly teaches that the same parity checks are performed and then the results of the words received in parallel are compared (and are identical if no error has occurred), see column 6, lines 1-8.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to adapt the memory of Richter to include the teachings of

Cloonan. This modification would have been obvious because one of ordinary skill in the art would have been motivated by the suggestion provided by Cloonan to provide serial communication of data at very high actual and effective data rates with high probabilities of detecting errors, see abstract, lines 1-3. Both Richter and Cloonan teach of redundant memory/data transfers that involve generating parity checks to determine the validity of the received data.

Further, it would have been obvious to one of ordinary skill in the art to use the parity of the entire digital word to determine if two received packets are without error. As noted above, it is not uncommon for two packets to contain the same data for different addresses. One method, as noted in claim 5 is to only compare the address portion. Along the same lines, one skilled in the art could just as easily implement the parity check to check the entire word (i.e. address and data portions). One skilled in the art would want to do this so as to offer better protection from erroneously comparing two unrelated words destined for the same address. By comparing the entire word (address and data) one skilled in the art can be more certain of the validity/invalidity of the received data.

As per claim 6,

Both of the above cited references, Richter and Cloonan, substantially teach, as combined above in claim 5, the limitations of claim 6.

With respect to the limitations of claim 6, Richter teaches of preventing the writing of data to memory when an error is detected, see column 6, lines 25-35. Further, Richter teaches of insuring that the memory module (104 of Figure 4) does not

utilize the signals received by completing execution of an instruction (i.e. a NOOP instruction), see column 6, lines 20-27. While Richter does not explicitly teach of the NOOP command causing the storage to be inhibited, Richter does suggest that when an error is detected, an instruction causes the storage to be inhibited. Further, a NOOP command is a command in which the instruction is to do nothing. In other words a NOOP command simply tells the device receiving the instruction to do nothing. The claimed limitations, however, read that a NOOP instruction is used to produce a certain action/desired output. Therefore the Examiner is viewing the NOOP instruction simply as an instruction causing the memory/data to not be written to memory. Once read in this light, it is clear that Richter teaches of a issuing an instruction to inhibit the writing to memory of data once the data is found to have an error.

As per claim 7,

Both of the above cited references, Richter and Cloonan, substantially teach, as combined specifically above in claims 3 and 5, the limitations of claim 7.

With respect to the limitations of claim 7, the limitations are identical to the limitations set forth in claims 3 and 5 with the exception that the causes of a NOOP instruction are combined.

Richter substantially teaches of a system where data is read from and stored in a memory, see abstract line 1, with the data having address/control portion, see the command address description in column 3, lines 20-35. Richter further teaches of a pair of controller sections that implement identical logic that controls the transfer of data into the memory, see column 5, lines 5-20. The parity checkers 127 and 128 of Figure

4 feed the control section 120 with the parity bits. The examiner is reading the parity checkers as section of a controller, where the controller includes the control 120 and the two parity checkers 127 and 128. The claimed controller is an obvious inclusion of the two parity checkers and the controller into a single unit.

Further, Richter teaches or write data port of a control section being connected to the memory, see line 164 of Figure 4, which controls the writing to the memory of the data in register 169. Richter further teaches of, when an input error is detected (i.e. the parity checks aren't equal), the control (or the checker) ensuring that the memory module (104 of Figure 4) does not utilize the signals received by completing execution of an instruction (i.e. a NOOP instruction), see column 6, lines 20-27.

Richter does not explicitly teach of the first port being connected to both sections or specifically of the parity of the address/control portion being used. Nonetheless, Richter does teach of preventing the use of erroneous signals by comparing the parity of the two signals and of preventing the use signals when an error is detected (i.e. the results of the parity checks do not match).

Cloonan, in an analogous art, teaches of a first port (reference 42 of Figure 2) feeding into/connected to two transmitters 60 and 80, which in turn feeds out to output bus 120. Cloonan also explicitly teaches that both copies of the data are generated from the same signal, i.e. input 42 of Figure 2. Further, Cloonan explicitly teaches that the same parity checks are performed and then the results of the words received in parallel are compared (and are identical if no error has occurred), see column 6, lines 1-8.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to adapt the memory of Richter to include the teachings of Cloonan. This modification would have been obvious because one of ordinary skill in the art would have been motivated by the suggestion provided by Cloonan to provide serial communication of data at very high actual and effective data rates with high probabilities of detecting errors, see abstract, lines 1-3. Both Richter and Cloonan teach of redundant memory/data transfers that involve generating parity checks to determine the validity of the received data.

Further, it would have been obvious to one of ordinary skill in the art to use the parity of a specific part of received data to determine if two received packets are without error. Specifically, it is not uncommon for two packets of data to have the same payload with different destinations. In this case, it would be obvious to one of ordinary skill to want to use the parity of the address section only to determine the validity of received packets. Further, it would have been obvious to one of ordinary skill in the art to also use the parity of the entire digital word to determine if two received packets are without error. As noted above, it is not uncommon for two packets to contain the same data for different addresses. One skilled in the art could just as easily implement the parity check to check the entire word (i.e. address and data portions). One skilled in the art would want to do this so as to offer better protection from erroneously comparing two unrelated words destined for the same address. By comparing the entire word (address and data) one skilled in the art can be more certain of the validity/invalidity of the received data. In view of both of the above methods, it is clear that one is geared

toward speed (checking the parity of the address/control takes less time than the entire word) and the other geared towards higher reliability (checking the parity of the entire digital word ensures that the correct/incorrect word is detected). One of ordinary skill would want to have both types of detection because the address/control checking disposes of errors quickly and the entire word checking is more exact in the detection of errors.

As per claim 8,

Both of the above cited references, Richter and Cloonan, substantially teach, as combined above in claim 7, the limitations of claim 8.

With respect to the limitations of claim 8, Richter teaches of preventing the writing of data to memory when an error is detected, see column 6, lines 25-35. Further, Richter teaches of insuring that the memory module (104 of Figure 4) does not utilize the signals received by completing execution of an instruction (i.e. a NOOP instruction), see column 6, lines 20-27. While Richter does not explicitly teach of the NOOP command causing the storage to be inhibited, Richter does suggest that when an error is detected, an instruction causes the storage to be inhibited. Further, a NOOP command is a command in which the instruction is to do nothing. In other words a NOOP command simply tells the device receiving the instruction to do nothing. The claimed limitations, however, read that a NOOP instruction is used to produce a certain action/desired output. Therefore the Examiner is viewing the NOOP instruction simply as an instruction causing the memory/data to not be written to memory. Once read in

this light, it is clear that Richter teaches of a issuing an instruction to inhibit the writing to memory of data once the data is found to have an error.

As per claim 9,

Richter substantially teaches of a system where data is read from and stored in a memory, see abstract line 1, with the data having address/control portion, see the command address description in column 3, lines 20-35. Richter further teaches of a pair of controller sections that implement identical logic that controls the transfer of data into the memory, see column 5, lines 5-20. The parity checkers 127 and 128 of Figure 4 feed the control section 120 with the parity bits. The examiner is reading the parity checkers as section of a controller, where the controller includes the control 120 and the two parity checkers 127 and 128. The claimed controller is an obvious inclusion of the two parity checkers and the controller into a single unit.

Further, Richter teaches of a write data port of a control section being connected to the memory, see line 164 of Figure 4, which controls the writing to the memory of the data in register 169. Richter further teaches of, when an input error is detected (i.e. the received signals or their parity checks are not equal), the control (or the checker) insuring that the memory module (104 of Figure 4) does not utilize the signals received by completing execution of an instruction (i.e. a NOOP instruction), see column 6, lines 20-27.

Richter does not explicitly teach of the first port being connected to both sections or of a checker comprising a parity generator. Nonetheless, Richter does teach of preventing the use of erroneous signals by comparing the parity of the two signals and

of preventing the use signals when an error is detected (i.e. the results of the parity checks do not match).

Cloonan, in an analogous art, teaches of a first port (reference 42 of Figure 2) feeding into/connected to two transmitters 60 and 80, which in turn feeds out to output bus 120. Cloonan also explicitly teaches that both copies of the data are generated from the same signal, i.e. input 42 of Figure 2. Further, Cloonan explicitly teaches that the same parity checks are performed and then the results of the words received in parallel are compared (and are identical if no error has occurred), see column 6, lines 1-8.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to adapt the memory of Richter to include the teachings of Cloonan. This modification would have been obvious because one of ordinary skill in the art would have been motivated by the suggestion provided by Cloonan to provide serial communication of data at very high actual and effective data rates with high probabilities of detecting errors, see abstract, lines 1-3. Also, both Richter and Cloonan teach of redundant memory/data transfers that involve generating parity checks to determine the validity of the received data.

Further, Richter teaches that depending on the inputs to the control, 120 of Figure 4, the write enable line, 164 will either be allowed or inhibited. Richter teaches of the equations that are used to determine whether a failure has occurred, see column 5, lines 55-65. These equations determine whether or not an input error has occurred and therefore perform equivalent to the parity generator of the checker. One skilled in the

art would see that the inputs cause the write enable (as a digital signal) as a 0 or 1 value with, i.e., 1 being allowed and 0 being inhibited. Still further, if the write enable is inhibited, there had to have been some kind of input error. As noted above, an error will inhibit write enable, in essence causing a 0, or inverted signal/bit, to be outputted. Similarly, if there are no errors present, a 1 will be outputted.

Still further, one skilled in the art could use the parity bit comparisons to determine if the packets are the same or different (see control unit 120 of Figure 4), or if the entire digital words are the same or different (see compare 125 of Figure 4).

As per claim 10,

All of the above cited references, Richter and Cloonan, substantially teach, as combined above in claim 9, the claimed limitations of claim 10.

With respect to the limitations of claim 10, it would have been obvious to one of ordinary skill in the art to send an inverted bit (i.e. 0 or inhibit the write enable) if the parity bits disagree or if the digital words disagree, both of which are indications that there has been an error in the input.

As per claim 11,

All of the above cited references, Richter and Cloonan, substantially teach, as combined above in claim 9, the claimed limitations of claim 11.

With respect to the limitations of claim 11, Richter further teaches of a data port for receiving the data and the address/control information, see Figure 3 where the data packet has address and data information. Still further, Richter, in Figure 4 teaches of an

address/control port connected to the memory, see Address IN port, on memory element 166 of Figure 4, and of a write port, see Data In of Figure 4.

As per claim 12,

All of the above cited references, Richter and Cloonan, substantially teach, as combined above in claim 9, the claimed limitations of claim 12.

With respect to the limitations of claim 12, it would have been obvious to one of ordinary skill in the art to send an inverted bit (i.e. 0 or inhibit the write enable) if the parity bits disagree or if the digital words disagree, both of which are indications that there has been an error in the input.

As per claim 13,

All of the above cited references, Richter and Cloonan, substantially teach, as combined above in claim 9, the claimed limitations of claim 13.

With respect to the limitations of claim 13, Richter teaches of a communication system between processors and memory, see column 1, lines 1-10 and of two way communication, see column 3, lines 1-5. Richter further teaches of an input port see the inputs to control 120 of Figure 4, for transmitting data from memory and of a read data port, see data out port of memory elements 166 of Figure 4, for reading data out of memory.

Further, Richter teaches that depending on the inputs to the control (checker), 120 of Figure 4, the write enable line, 164 of Figure 4, will either be allowed or inhibited. Richter teaches of the equations that are used to determine whether a failure has occurred, see column 5, lines 55-65. These equations determine whether or not an

input error has occurred and therefore perform equivalent to the parity generator of the checker. One skilled in the art would see that the inputs cause the write enable (as a digital signal) as a 0 or 1 value with, i.e., 1 being allowed and 0 being inhibited. Still further, if the write enable is inhibited, there had to have been some kind of input error. As noted above, an error will inhibit write enable, in essence causing a 0, or inverted signal/bit, to be outputted. Similarly, if there are no errors present, a 1 will be outputted. While not explicitly disclosing an inverter, Richter does teach of allowing or inhibiting the write enable line. Since one signal will be high and one will be low, it is clear that an inverter, or equivalent, can be used to do so.

Still further, one skilled in the art could use the parity bit comparisons to determine if the packets are the same or different (see control unit 120 of Figure 4), or if the entire digital words are the same or different (see compare 125 of Figure 4). Further, it would have been obvious to one of ordinary skill in the art to use a selector, or equivalent, to choose between sending an inverted (i.e. 0 and hence inhibiting) signal or a enable (i.e. 1) signal out if the parity bits or digital words were the same (enable) or different (inhibit).

As per claim 14,

All of the above cited references, Richter and Cloonan, substantially teach, as combined above in claim 9, the claimed limitations of claim 14.

With respect to the limitations of claim 14, it would have been obvious to one of ordinary skill in the art to send an inverted bit (i.e. 0 or inhibit the write enable) if the

parity bits disagree or if the digital words disagree, both of which are indications that there has been an error in the input.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Aoyanagi et al. Japanese Patent Abstract, Publication No. 57-092499

This reference teaches of preventing erroneous operations by calculating parity bits and comparing those bits. If the bits are not identical, then an inhibition signal causes the data to be retained in memory (and not outputted).

b. Murai U.S. Patent No, 5,033,050

This reference teaches of inhibiting writes if the data fails parity.

c. Gupta et al. U.S. Patent No. 5,475,858

This reference teaches of inhibiting the transfer of the address and data if a parity error is detected.

d. Honma et al. U.S. Patent No. 5,412,662

This reference teaches of inhibiting the writing to memory through the use of a write enable signal.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Marshall S Eng whose telephone number is (703) 305-4638. The examiner can normally be reached on M-F, 9:00 am to 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

ME

mse

Gary J. Lamarre for

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